INFORMATION DISCLOSURE CITATION PTO-1449	CUSTOMER NUMBER 45114	ATTORNEY'S DKT NO. H1419	APPLICATION NO. 10/633,504
		APPLICANT(S) Bin Yu et al.	
		FILING DATE August 5, 2003	GROUP 2826

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2002/0011612A1	01/31/02	Hieda	257	262	
	2003/0102497A1	06/05/03	Fried et al.	257	255	
	2004/0110331A1	06/10/04	Yeo et al.	438	199	
	5,391,506	02/21/95	Tada et al.	437	41	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	F. Daugé et al., "Channels Separation in FINFETs", ULIS'2003 Workshop, Udine, March 20-21 2003, 20 pages, XP002321769
	N.H.E. Weste et al., "Principles of CMOS VLSI Design", Addison-Wesley, XP002321770, pages 140-141, 1988
	J. Park et al., "Pi-Gate SOI MOSFET", IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pages 405-406, XP001099966
	M. Lemme et al., "Influence of channel width on n- and p-type nano-wire-MOSFETs on silicon on insulator substrate", Microelectronic Engineering, Vol. 67-68, June 2003, pages 810-817, XP004428954

EXAMINER	DATE CONSIDERED
Tetsu Abraal	7/8/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).